CHIPWRIGHTS
Visual Signal Processors

Application Note: PCB Layout Guidelines for the ChipWrights CW4512

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Abstract:

This Application Note details the guidelines for creating a Printed Circuit Board (PCB) for the ChipWrights Visual Signal Processors CW4512.

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2 Introduction

This document intends to give general guidelines for placing and routing the ChipWrights 256 fpBGA VISP. Good design practices should always be followed when designing any high-speed device and the CW4512 is no exception to this rule.

3 PCB Layout Guidelines for the ChipWrights CW4512

3.1 Recommended land pattern for the 256-pin BGA

In order to make room to place bypass components as close as possible to the core power and ground pins it is advisable to use the following via pattern for the 256-pin BGA device:

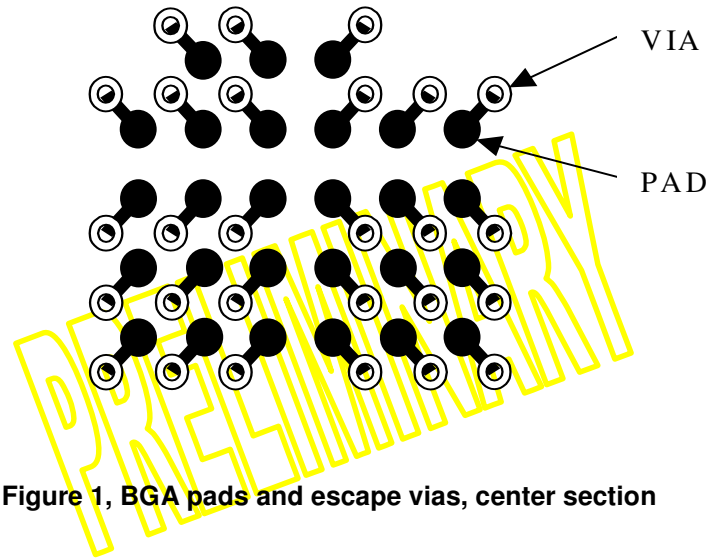

Figure 1, BGA pads and escape vias, center section

Figure 1 shows the center of an array of BGA pads, with a connect line (stringer) and a via for each pin on the 256-pin device. BGA pads and the stringers only appear on the layer of the PCB that the component itself is placed on. The vias are generally drilled completely through the PCB and are the main concern for routing of lines. As you will notice from the suggested array, the 16x16 device is essentially quartered into four 8x8 arrays. This allows for a wide routing channel in the center of the device as well as bypass cap component placement on the bottom side of the PCB. Placing bypass capacitors in the center of the device allows optimal performance for high frequency bypass (.01 µf to .1 µf).

For power and ground pads, it is very important to avoid sharing vias. Each power and ground pin should have its own via whenever possible. No more than two pads should ever share one via, although sharing vias between components on opposite sides of the board is acceptable.

3.2 Via size

In congested areas (such as under the fp256 BGA) the via geometry must be selected to insure a minimum of 5 mils clearance between the keepouts for adjacent vias. Said another way, maintaining at

least 5 mils of copper on power and ground planes between all escape vias is required for the CW4512.

As an example, with a 39mil (1mm) pad pitch such as that of the CW4512, using a 12 mil drill size with a 24 mil annular ring leaves 15 mils between the rings of adjacent vias. This allows a 5 mil channel for traces and power planes with 5 mils of clearance on either side. Even better, by reducing or eliminating the annular ring for vias on plane layers, an even larger channel is possible.

This low-impedance requirement applies to both the core supply and the IO supply. If having separate planes for the two supplies would be prohibitive, it is acceptable to split a single power plane into sections under the CW4512, provided no section has any point with a width less than 150 mils. Figure 2 shows an example of a successful split-plane design.

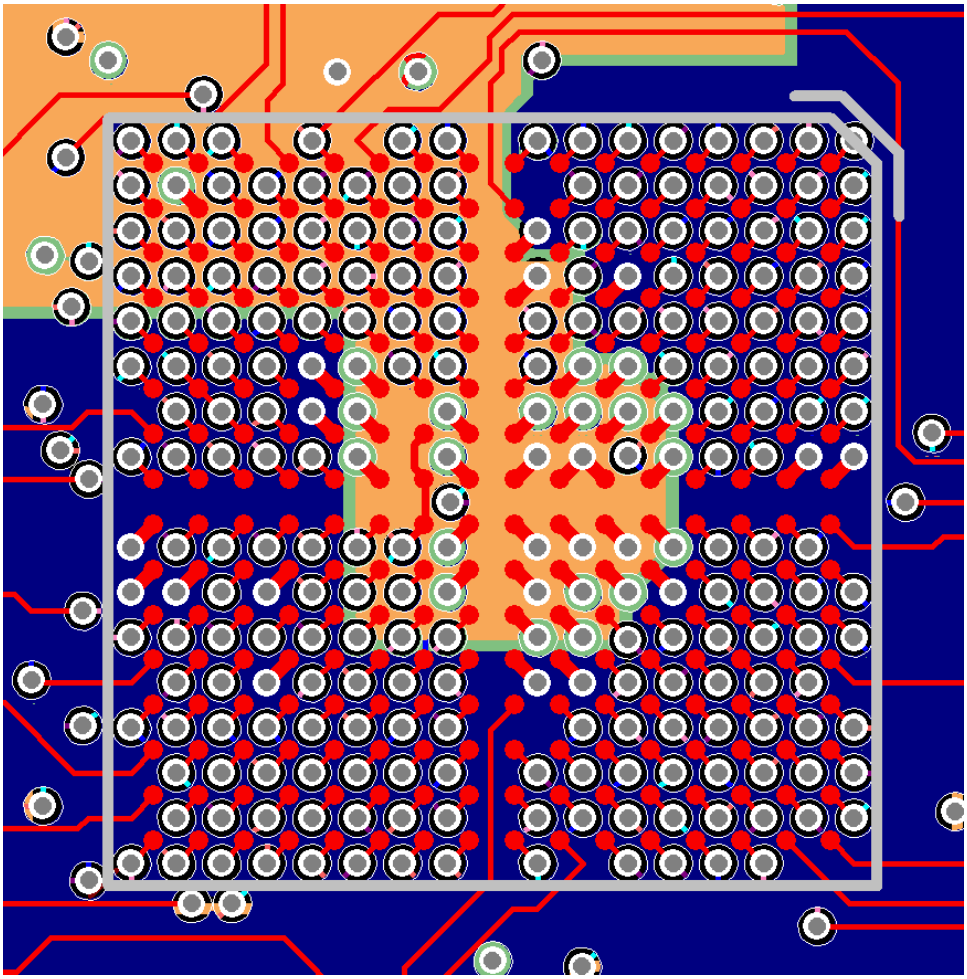

Figure 2, Orange represents VDDE, Blue represents VDDI

Blind and/or buried vias may also be used to obtain more copper on the plane layers if cost is not a concern.

3.3 Considerations for memory signals

Transmission line effects will adversely influence the signal integrity of the high-speed control lines and busses on the CW4512. In particular special attention should be paid to the SDRAM clock (MCLK). Series termination is recommended with typical values of 22 to 44 ohms depending on the PCB impedance. The bi-directional data lines are normally not terminated since they would have to be source and destination matched.

Series termination and MCLKIN connection methods are as shown below. The trace length from the resistor to the MCLKOUT pin should as short as possible.

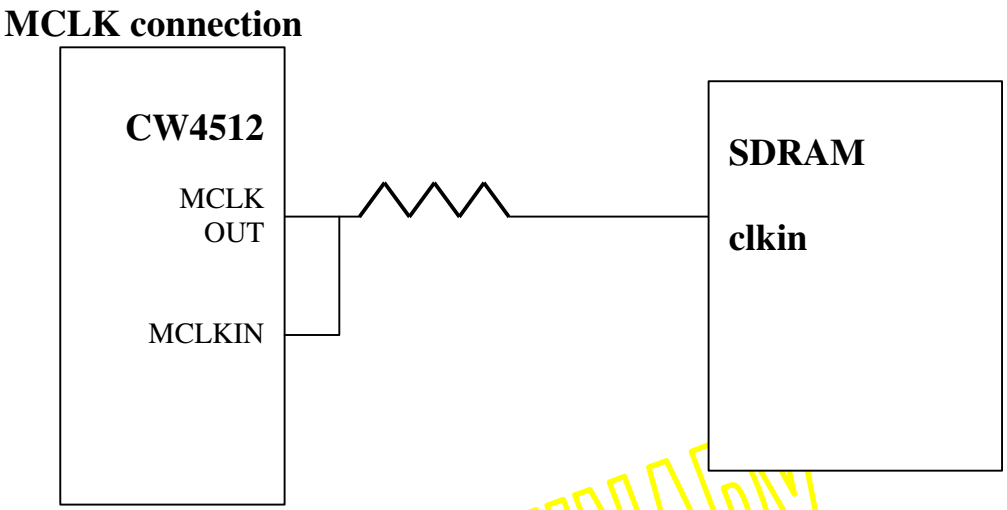

Figure 3

ChipWrights recommends matching all of the trace lengths to the SDRAM to within 500 mils, and placing the SDRAMs as close as possible to the VISP to minimize the overall length of the traces between the devices. It is possible to route the devices with as little as 1” of trace on each signal.

3.4 VDDI and VDDE and ground planes

When designing a power (VDDI or VDDE) or ground plane, it is important to maintain as much area in the plane as possible. This includes the thickness of the plane. ChipWrights recommend using 1-ounce copper for all power and ground planes.

Single ground planes that are unbroken between the VISP and the SDRAM are required.

Low impedance paths to the current source (voltage regulator or switching power supply) should be maintained. Traces should never be used to carry Voltage supplies to the ASIC, as they will have a measurable inductance and will contribute to the noise in the system.

If there is a connector/cable in the power subsystem design it is advisable to use as many contacts as possible to carry the power and ground lines to the VISP. A minimum of 50 mils trace width should be used in feeding any of the power planes, and multiple, large vias should be used.

3.5 More on Bypass

Capacitor construction is also important to consider when choosing bypass caps. Ceramic caps are a good choice because of their size, frequency response and cost. Place as many bypass caps as possi-

ble directly under or adjacent to the VISP. Package sizes as small as 0402 may be needed to accomplish this.

A rule of thumb of 1 bypass cap per power pin is suggested, although difficult in practice. Small value bypass should be placed under the BGA power pads (as previously discussed), larger values can be placed outside the VISP, and very large bulk caps should be placed at the output of the voltage regulator itself or near the power connector if one is used. For all supplies, having a large area of copper power plane over a continuous ground plane also provides useful bypassing at the highest frequencies.

Higher value capacitance in the range of 1 to 10 µf (and above) caps, should be used for lower frequency bypassing and can be placed outside the periphery of the BGA. When designing switching power supplies, the output of these devices require high value capacitors (100 µf or larger) with very low ESR to dampen the switching transients of these regulators.

An example of good high frequency bypass cap placement is shown in figure 4 below.

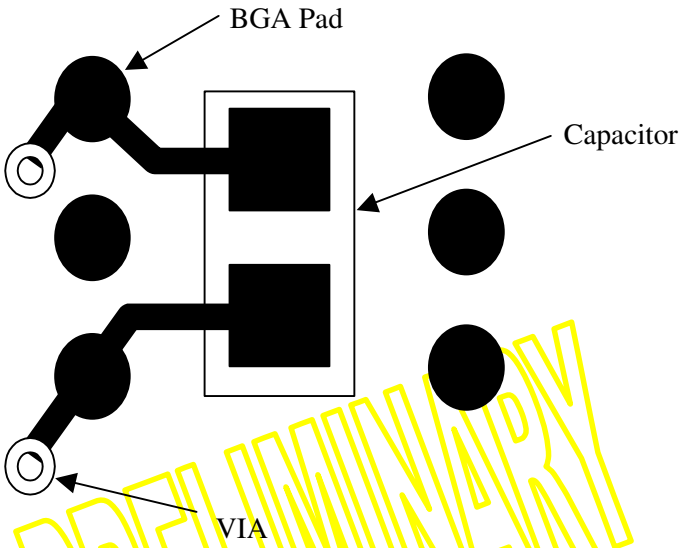

Figure 4

By minimizing the length of the trace to the power and ground pins and maximizing the width of the traces to the component's vias, this approach will provide the optimal component placement and routing. Long traces to bypass caps placed far away from the power pins are of limited value since the trace inductance now becomes a factor in the ability of the capacitor to supply energy in the short time scales in which it is required.

If possible, each power pin should have a corresponding capacitor placed as shown. Physically this is not always possible but it is the ideal situation.

4 Summary

These guidelines are provided to minimize the risk of poor performance arising from the layout of the Printed Circuit Board. Poor power integrity in high-speed DSP systems is a frequent cause of errors and crashes, which can be very difficult to debug and have an inherent cost which far exceeds that of doing the design carefully the first time. Such crashes may be indistinguishable from a software bug without extensive investigation. Strict adherence to these guidelines is advised.

5 Limitations and Restrictions

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6 Revision History

Revision	Date	Comment
0.00	5-Aug-04	Initial Draft release
0.10	5-Aug-04	Added example layout, other changes throughout.
0.20	23-Aug-04	Minor corrections.

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